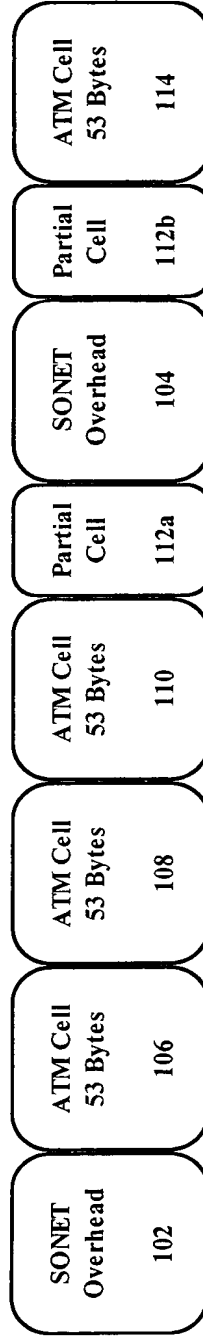


Fig 1
(PRIOR ART)

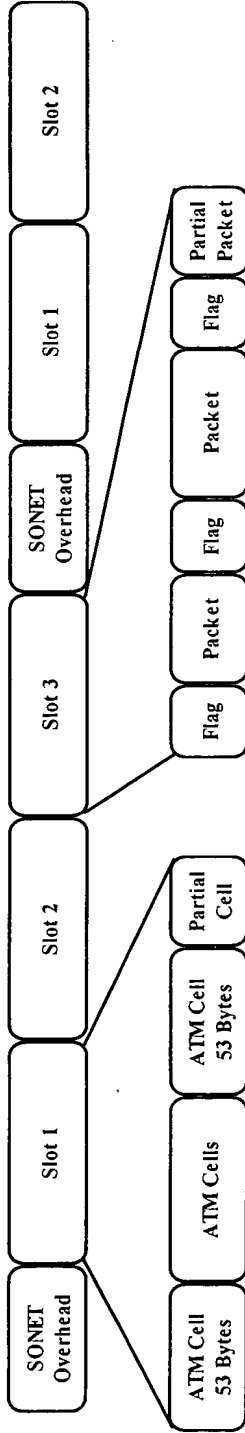


ATM Cell
53 Bytes

114

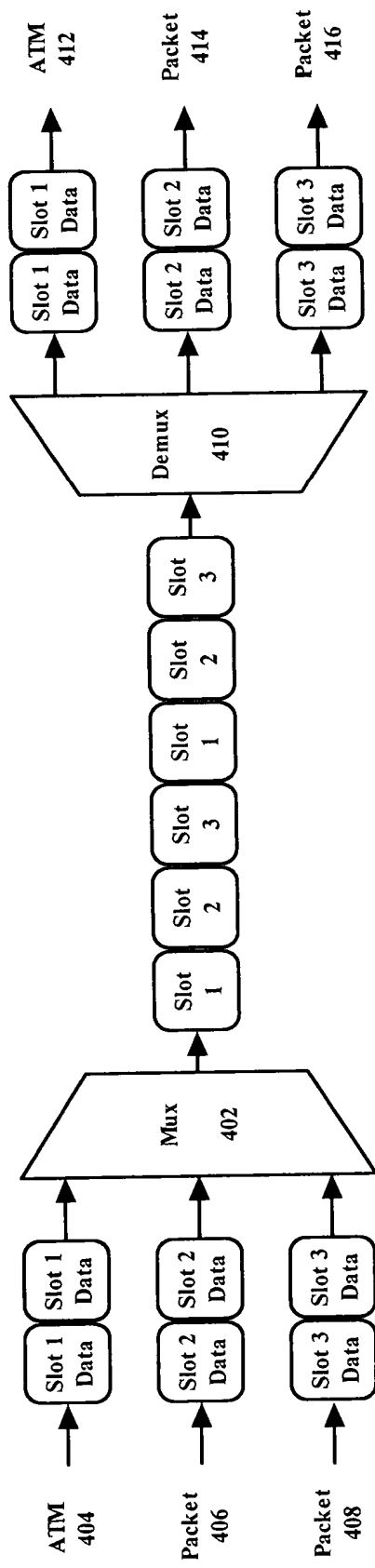
fig 3

(PRIOR ART)



(PRIORITY)

fig 4



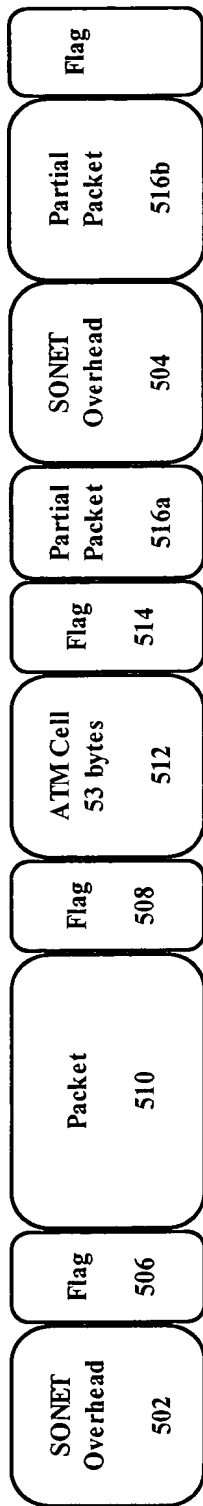


Fig. 5A

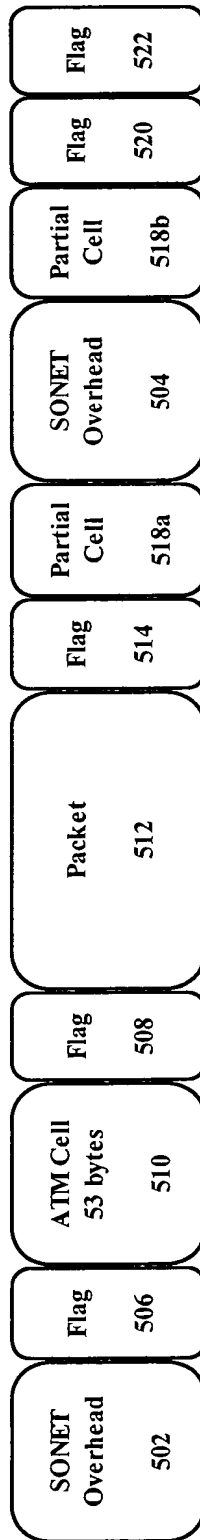


Fig. 5B

Fig 6
(Prior ART)

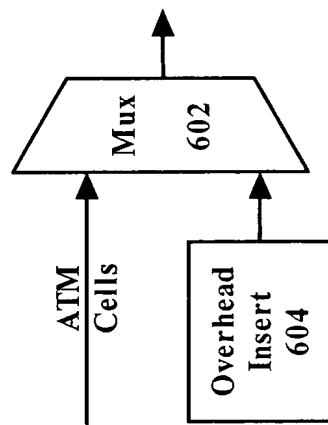


Fig 7
(PRIOR ART)

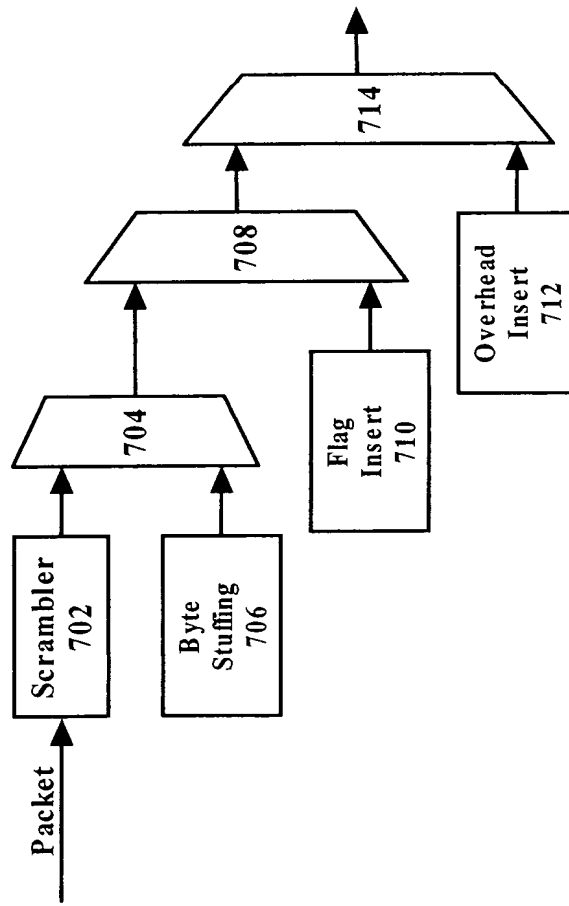
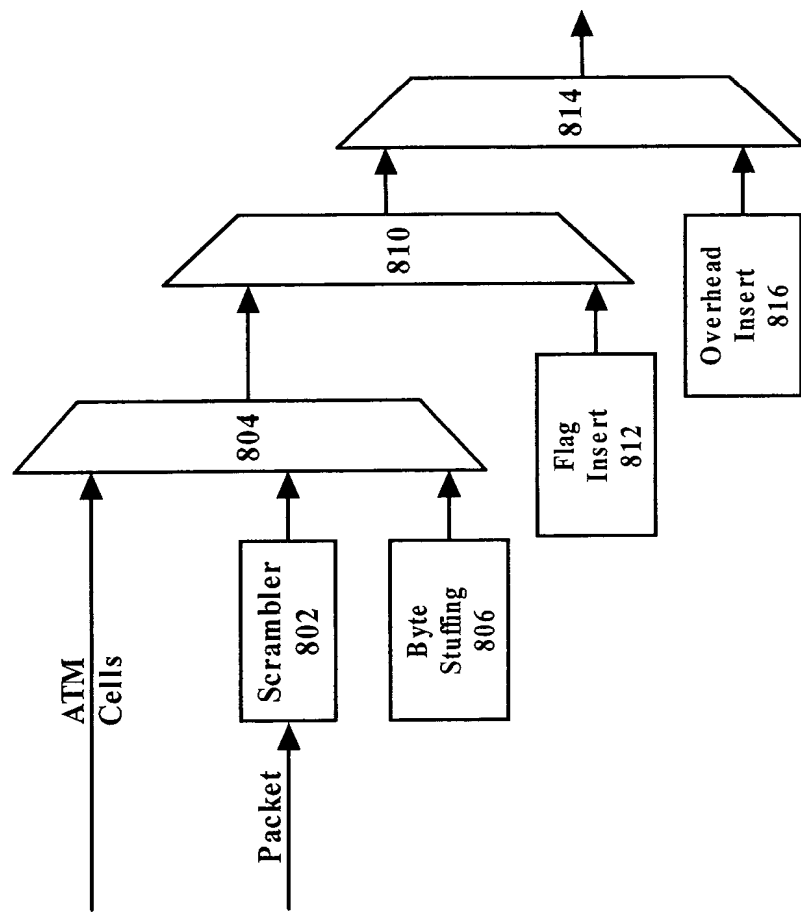


Fig 8



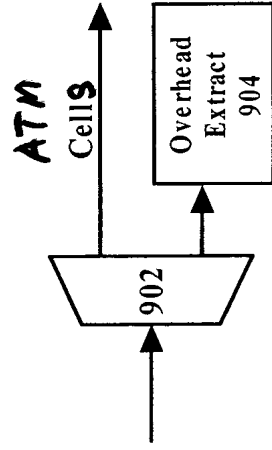


Fig. 9
(Prior Art)

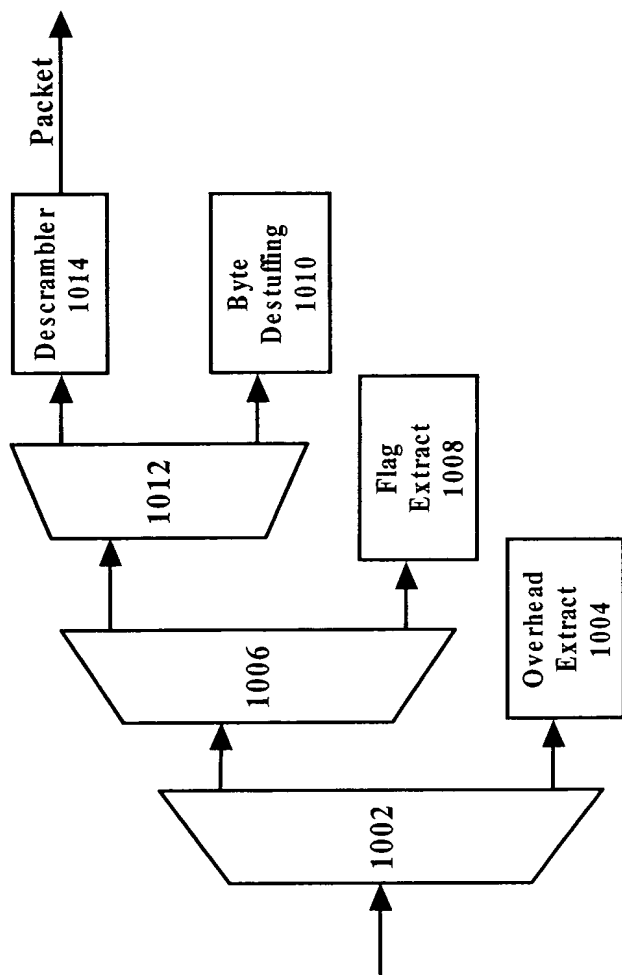


FIG. 10 (PRIOR ART)

FIG. 11 is a block diagram of a packet processing system.

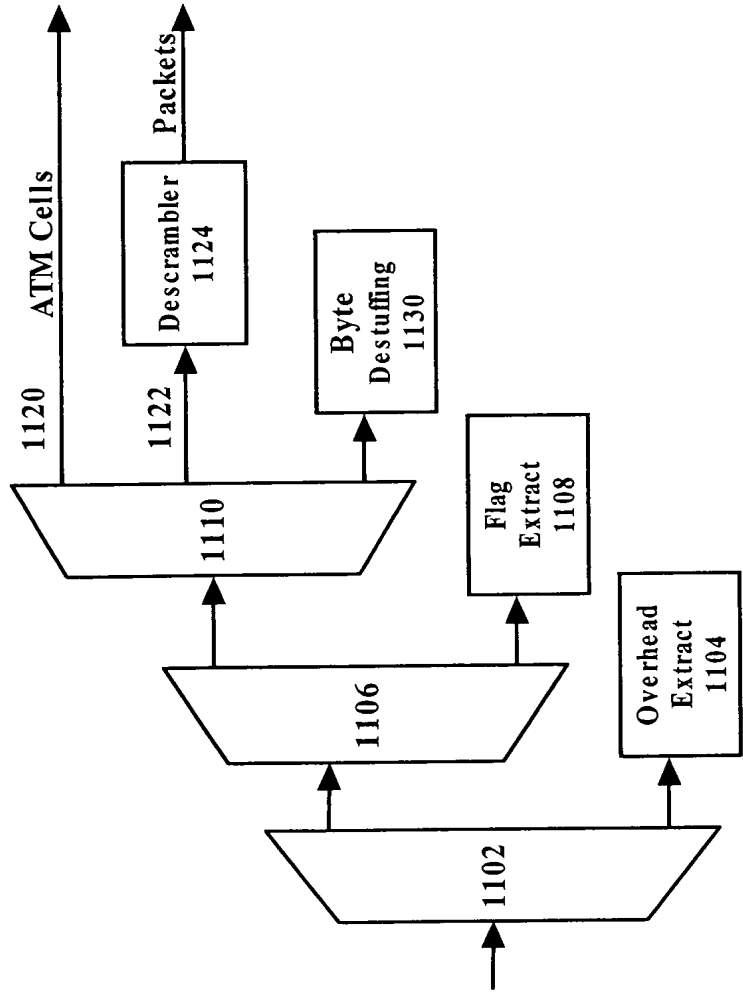


Fig. 11

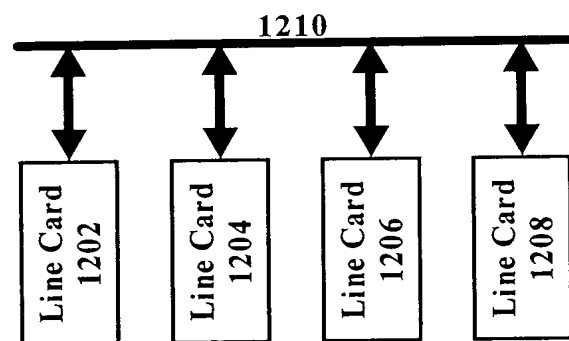


Fig. 12

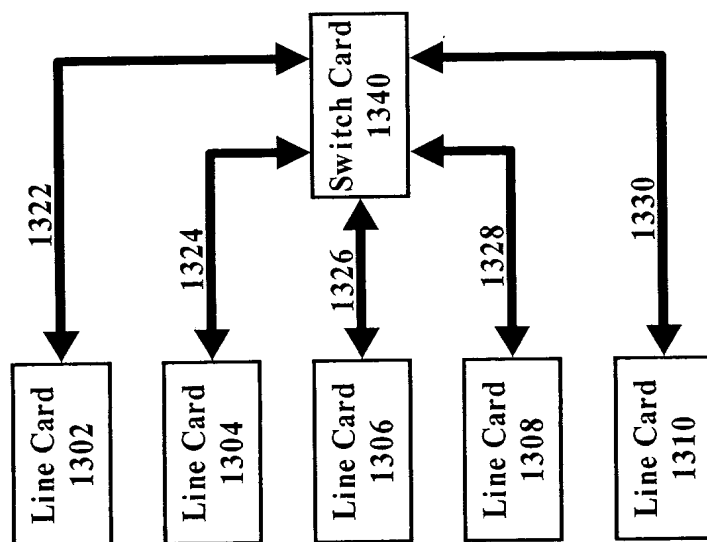


Fig. 13

